TLS-Dicing™: A Novel Laser-based Dicing Approach for Silicon Carbide Power Devices

Introduction

This paper will give an overview of the potential of TLS-Dicing™ for SiC-based semiconductor products. A typical power device wafer with full backside metallization, polyimide on the top side, and metal structures in the dicing streets was separated by using TLS-Dicing™. A high yield count in combination with very high edge quality was demonstrated. The dicing costs per wafer were significantly reduced.

Challenges with Dicing SiC Power Devices

Silicon carbide (SiC) is a crystalline compound of silicon and carbon. It possesses certain qualities such as high charge carrier mobility, high strength, hardness, and high thermal conductivity. Due to these characteristics, SiC is considered a replacement material for silicon (Si)-based semiconductors in the electronics industry in certain applications, including power devices, light emitting diodes (LEDs), and sensors for harsh environments.

The traditional technique for separating SiC devices from wafer form is mechanical blade sawing. This method involves a very fast rotating foil with abrasive particles to remove the wafer material. Due to the hardness of SiC (Mohs scale 9.2), blade sawing suffers from low feed rate and high wear of the diamond coated dicing blade, resulting in the risk of uncontrolled tool breakage during the dicing process. In addition, blade sawing can result in chipping and delamination at the edge of the die (Figure 1). An advanced version of this approach is ultrasonic vibration-supported mechanical sawing, which provides slightly higher dicing speed (10-20 mm/s), but in principle it has the same limitations. With the upcoming transition of SiC wafer sizes from 4-inch to 6-inch diameters, mechanical blade dicing will reach its limit since the cumulated street length more than doubles and is beyond the ability of one saw blade to completely cut. In this situation, the blade would either have to be changed while the wafer is in work-position or—in the worst case scenario—the blade will break during the middle of the dicing process and damage the wafer.

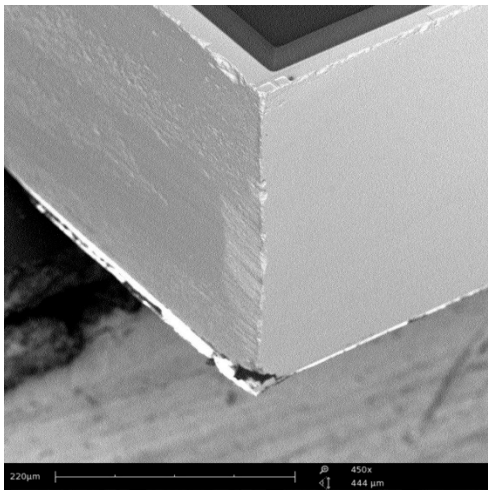

Figure 1: SiC die edge after mechanical dicing shows chipping and delamination defects [1]

TLS-Dicing™ Technology Overview

Thermal Laser Separation (TLS-Dicing™) is a fast, clean and cost-effective alternative for separating SiC-based semiconductor products. It has many advantages compared to competing technologies such as blade sawing and laser ablation:

- High separation speed (up to 300 mm/s for SiC) resulting in a throughput of 10 wafers per hour (assuming a 4-inch wafer with 2-mm die size)
- Very smooth edges (avoids increased leakage current of vertical diodes by leaving the p/n-junction undamaged)
- Nearly no chipping and micro cracks for less breakage
- Thin backside metal on the chip is separated without damage
- No tool wear
- Low cost of ownership due to no tool wear and nearly no consumables
- Zero kerf cleaving for reduced street width

The TLS-Dicing™ process uses thermally induced mechanical stress to cleave brittle semiconductor materials such as SiC, Si, Germanium (Ge) and Gallium Arsenide (GaAs). A laser heats up the solid, brittle material and generates a zone of compressive stress, surrounded by a zone of tangential tensile stress pattern (Figure 2a). A second cooled zone with a minimum distance to the first one induces a tangential tensile stress pattern (Figure 2b). The resulting tensile stress in the overlaying region of both stress patterns has a local maximum that is sharply focused and has a clear orientation (perpendicular to the street), and thus is able to open and guide the crack tip through the material. (Figure 2c).

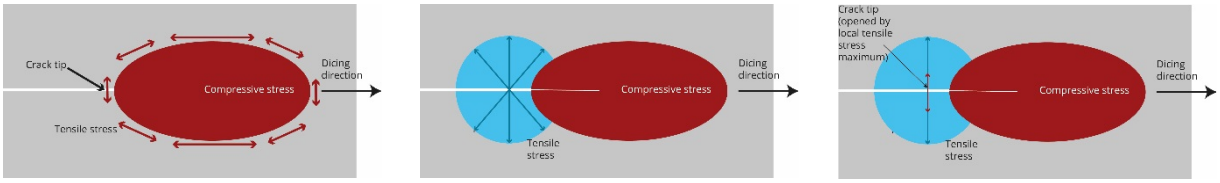

Figure 2a) tangential stress around the compressed zone *(b) tensile stress in cooled zone* *c) overlaying stress opens and guides the cleave*

TLS-Dicing™ itself is always a one-pass process that separates the whole thickness of the wafer at once. The starting point is given by a shallow scribe that is either local or continuous at the wafer's surface. The local scribe is preferred to ensure the highest bending strength and least particle generation. On the other hand, the continuous scribe offers best results for products with metal in the street and improves the straightness of the cleaving process.

Due to the fact that TLS-Dicing™ is a cleaving process, the die edges are smooth and free of remaining stress or micro cracks and chipping zone (Figure 3). Any reduction in bending strength as a result of the dicing process is significantly lower compared to ablative laser technologies. In addition, the backside metal is separated with no delamination or heat affects.

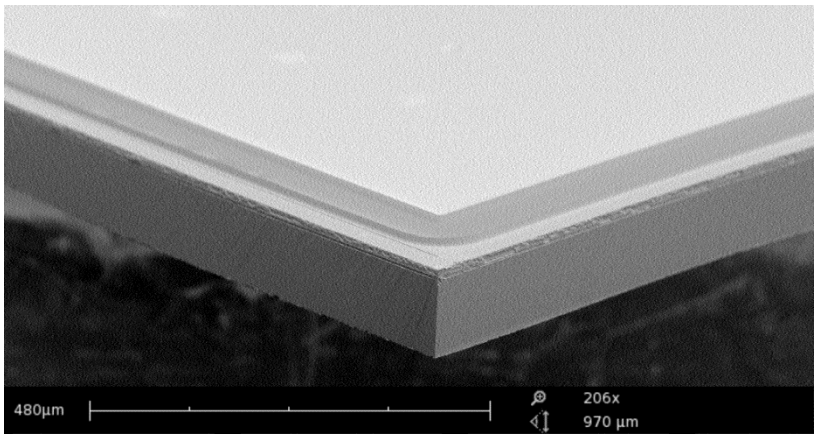

Figure 3: SiC die edge after TLS-Dicing™ process shows smooth edges and no micro cracks or chipping

TLS-Dicing™ Yield Case Study

To demonstrate the benefits of 3D-Micromac's TLS-Dicing™ technology, we conducted a case study evaluating the impact of TLS-Dicing™ on SiC device yields.

Application set-up

The wafer separation was done with a microDICE™ system using TLS-Dicing™ technology. The processed 4-inch wafer had a thickness of 110 µm and a thin silver-type backside metal stack. The streets were covered with several metal test structures. The active zone of the dies were protected by a Polyimide coating. On front side of the wafer, the outer part of the edge exclusion zone was covered by a ring of metallization and polyimide coating. Due to customer requirements, we simulated larger dies by building 3 by 3 die-clusters of smaller dies. For this reason only every third street was diced (Figure 4)

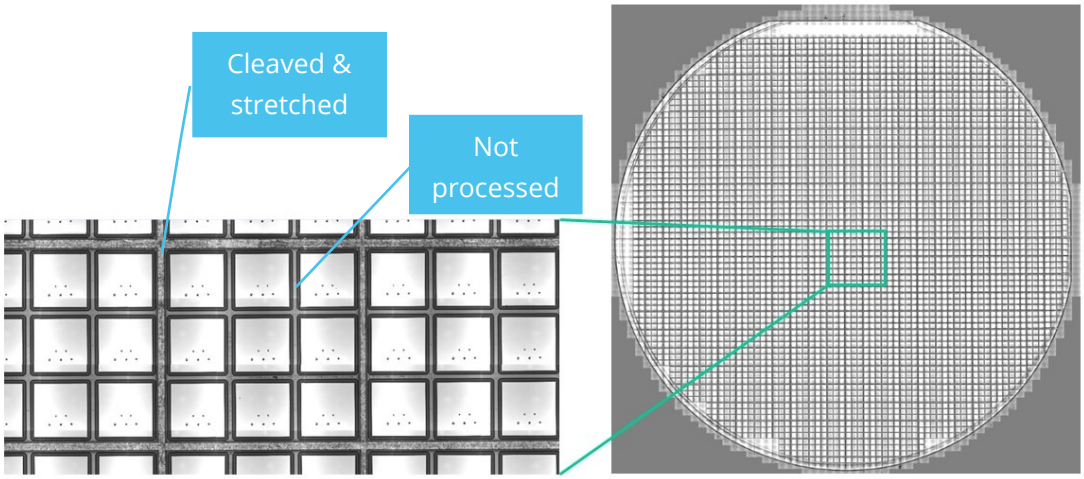

Figure 4: Whole wafer was diced, target die size was simulated by 3 by 3 clusters of smaller dies

As described earlier, each cleave needs a defined starting point in the form of a local initial scribe. To remove the reflecting metal structures in the street, a shallow continuous soft scribe along the entire street length was applied. The scribing laser is a 532 nm short-pulsed laser with a Gaussian beam

profile. Scribing speeds of 50 mm/s up to 200 mm/s were achieved. The lower the scribing speed, the smaller the heat affected zone of the polyimide cover layer and the particle pollution. Further investigations have shown that comparable scribing results can be achieved with less expensive near infrared (NIR) laser sources. A z-axis autofocus was used to obtain a smooth scribing line. The cleaving itself was realized by a 200 W continuous wave (cw) laser with near infrared (NIR) wavelength. The consumption of cooling liquid (DI-water) was below 10 ml/min.

Application results

TLS-Dicing™ was able to separate all chips without chipping and micro cracks (Figure 3). There is nearly no thermal impact of laser machining to the polyimide cover layer. No washing or cleaning and no protective coating was applied – a significant advantage in terms of operation costs. The separation of the backside metal was very smooth and without any delamination (Figure 5). This is important for minimizing problems during die mounting on the heat sink.

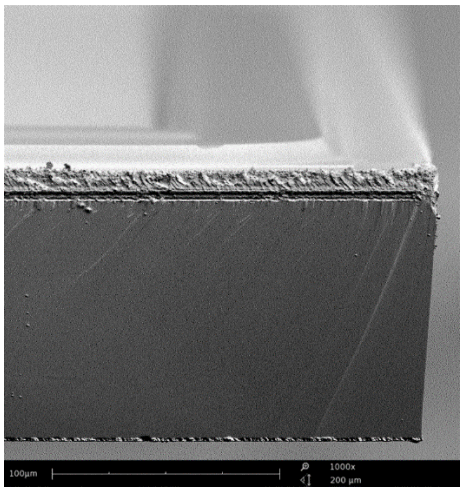

Figure 5: Smooth separation of backside metal (with the typical 4-degree off orientation visible).

The applied continuous scribe was used to open the metal structures without any impact on the bulk material after cleaving (Figure 6).

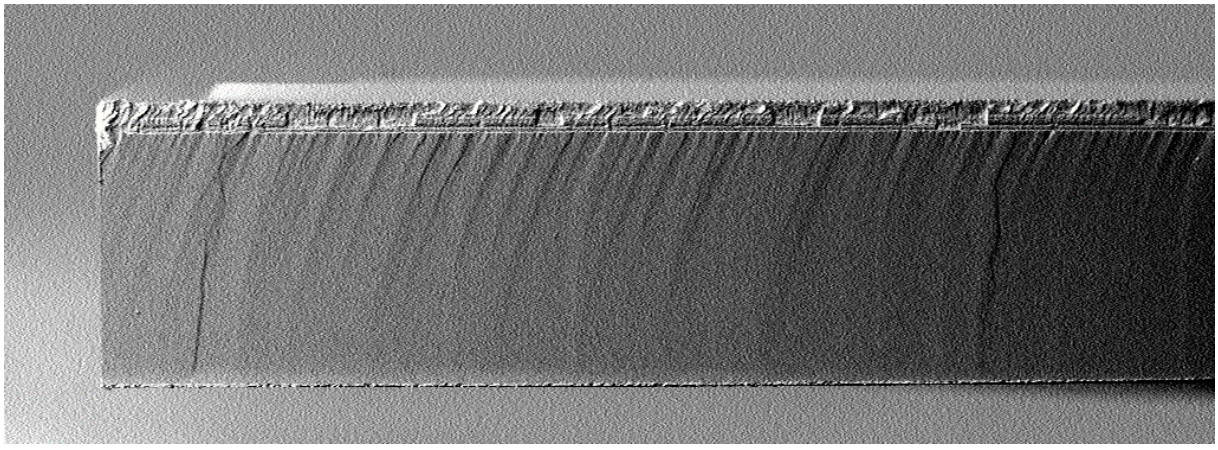

Figure 6: Effect of metal in the dicing street. Separation is successful with minor impact on straightness as indicated by the Wallner lines.

Yield Impact

The processed wafer was analyzed for defects and yield using a high-resolution optical inspection tool. This inspection method was adopted from a best practice of an industrial SiC device manufacturer. Yield consideration only includes dies inside the edge exclusion zone. The average yield value for this application is significantly higher than 98%. The observed defects and deviations have been categorized (Table 1). Nearly all of the defects are located in the edge exclusion region.

Defect Category	**Yield %**
perfect	97,97
minor straightness deviation	0,94
major straightness deviation	0,23
cleave failure by outer metal ring	0,83
Total Yield (all usable dies)	**98,91**

Table 1: Resulting average yield and yield losses by categories.

A noted characteristic pattern of the cleaving process was a short, local cleave dislocation, perpendicular to the edge of the wafer. In all cases, this deviation was limited to the edge exclusion region (see Figure 7) and can be ignored for yield calculation.

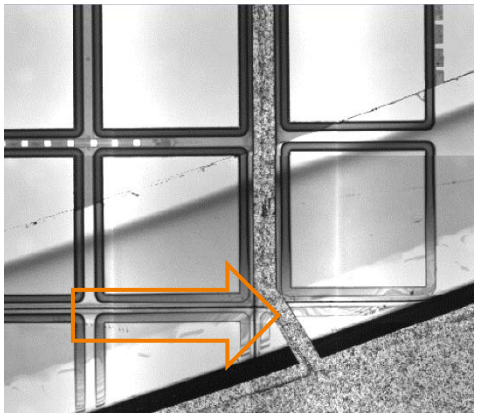

Figure 7: Perpendicular cleave exit at the wafer's edge, which is not yield relevant due to residing in the in-edge exclusion zone

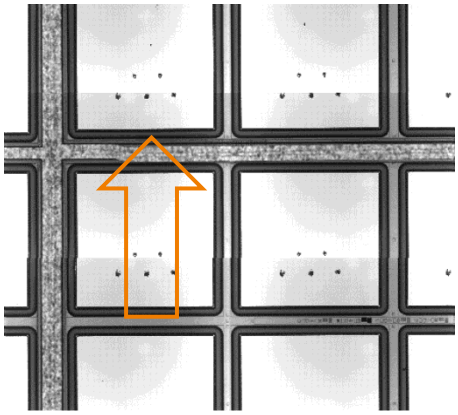

Figure 8: Sample for minor deviation with no influence on the electrical function

For a few chips, the cleave was not perfectly straight, but the deviation never reached the active area of any die (see "minor straightness deviation" in Table 1, and Figure 8).

In an even rarer occurrence, the cleave touched the active die area (see "major straightness deviation" in Table 1). A potential source of this is an overlaying internal stress pattern.

In this case study, the wafer had a massive metal and polyimide ring in the edge exclusion area on the top side of the wafer, which was built into the design rules by the manufacturer. The influence of this ring was visible and caused damage to a few die behind the edge exclusion (see “cleave failure by outer metal ring”). This error pattern can easily be avoided by implementing a laser clearing step comparable to the metal pattern opening in the dicing streets. Alternatively, this clearing step can be avoided by modifying the design rules to exclude any outer metal rings.

Conclusion

TLS-Dicing™ is a completely new approach for separating brittle materials at high throughput, low cost, and with high-separation quality. The cleaving principle shows unique advantages for SiC-based products with backside metallization, such as power devices. The case study highlighted in this white paper demonstrated a very high separation yield of 98.9%. This is an average value for a small batch of 4-inch SiC product wafers with backside metal, front side metal in the dicing street, and polyimide on the dies. As an outcome of this case study, it is suggested to either avoid designing in the metal ring, or take a less restrictive approach and remove the metal ring by implementing an additional laser clearing step. In both cases, the expected yield will increase an additional 0.8% (to a total yield count of 99.74%). Dies from a comparable wafer have been packaged, and after thermo-cycling only one out of 106 dies failed the leakage current test. The cause of this defect is believed to be unrelated to the TLS-Dicing™ process.

Furthermore, TLS-Dicing™ has demonstrated a significant improvement in terms of cost per wafer. A typical mechanical sawing process wears one saw blade per wafer due to the enormous hardness of SiC. To match the throughput of the TLS process, an investment in nine times more mechanical standard sawing tools is required. The overall cost per wafer will reach up to 35 € per 6 inch wafer for mechanical sawing but only 2.40 € per 6-inch wafer for the TLS system.

TLS-Dicing™ has demonstrated unique advantages for SiC-based power devices. Investigations and developments for other applications and materials (including silicon) are in preparation. For example, the ability to cleave without any particle generation could be an interesting option for flip-chip applications, such as MEMS and 3D-packaged wafers with solder bumps.

[1] Karl O. Dohnke et al., Comparison of different novel chip separation methods for 4H-SiC; Materials Science Forum Vols 821-823 (2015) pp 520-523